

## CLAIMS

We claim:

1. A decoupling capacitor, comprising:

a fixed resistance in series with said capacitor, said capacitor formed by a polysilicon layer and a diffusion layer, said fixed resistance formed by contacts connecting said polysilicon layer to a first voltage level buss and said diffusion layer to a second voltage level buss; and

said contacts being of location and quantity for limiting defect current while allowing said capacitor to function at a frequency sufficiently high to suppress noise on said first and second busses to a value which achieves bus stability.

2. The decoupling capacitor of claim 1, further comprising:

15           said contacts including a first set of contacts to a  
16           first voltage and a second set of contacts to a second  
17           voltage;

18           a defect leakage current limiting path including said  
19           first set and said second sets of contacts separated by  
20           a distance optimized to cause a defect shorting said  
21           polysilicon gate to said substrate to force defect  
22           current to travel from said first set of contacts  
23           through a section of the substrate, then to the  
24           polysilicon through the defect, and then along the rest  
25           of the polysilicon gate to said second set of contacts.

1       3.    The decoupling capacitor of claim 2, further  
2       comprising:

3           said first set of contacts and said second set of  
4           contacts determined in number and location to provide  
5           preselected minimum and maximum resistance values  
6           between said first and second sets of contacts, said  
7           minimum resistance value for achieving a preselected  
8           maximum leakage current through any defect site in said  
9           polysilicon layer, and said maximum resistance value

10           for achieving a preselected overall decoupling RC  
11           factor sufficient for a minimum RC network bandwidth.

1     4.    The decoupling capacitor of claim 3, further comprising  
2     providing said first and second sets of contacts in  
3     sufficient number to effectively achieve total contact  
4     resistance less than 10% of combined sheet resistance of  
5     said diffusion and polysilicon layers across a distance  
6     separating said first and second sets of contacts.

1     5.    The decoupling capacitor of claim 2, further comprising  
2     providing N pairs of contacts in said sets of contacts and  
3     placing said first and second sets of contacts separated by  
4     a distance K sufficient to achieve a leakage limiting  
5     resistance of R and a bandwidth limiting resistance of  $R/2$ .

1     6.    The decoupling capacitor of claim 2, further comprising  
2     providing a technology-dependent number of contacts selected  
3     in number sufficient to achieve total contact resistance  
4     less than 10% of combined sheet resistance of said diffusion  
5     and polysilicon layers across a distance separating said  
6     first and second sets of contacts.

1        7. A method for determining the number and position of  
2        contacts in a decoupling capacitor including a polysilicon  
3        layer and a diffusion layer, comprising:

4                determining a maximum allowable defect current  $I$  for  
5                IDDQ testing of said capacitor;

6                determining a minimum sheet resistance  $R$  to achieve  
7                said defect current  $I$ ;

8                determining minimum distance  $K$  between first and second  
9                sets of said contacts to achieve said minimum sheet  
10               resistance  $R$ ;

11               determining number of said contacts  $N$  in said sets of  
12               contacts to provide sufficiently low contact resistance  
13               to assure said minimum sheet resistance  $R$  dominates  
14               total resistance between said first and second sets of  
15               contacts; and

16               providing in said decoupling capacitor contact sites of  
17               sufficient area to accommodate  $N$  said contacts with

18           said first and second sets of said contacts separated  
19           by at least distance K.

1       8.    A program storage device readable by a machine,  
2       tangibly embodying a program of instructions executable by a  
3       machine to perform method steps for determining the number  
4       and location of contacts in a decoupling capacitor including  
5       a polysilicon layer and a diffusion layer, said method  
6       comprising:

7           determining a maximum allowable defect current I for  
8           IDDQ testing of said capacitor;

9           determining a minimum sheet resistance R to achieve  
10          said defect current I;

11          determining minimum distance K between first and second  
12          sets of said contacts to achieve said minimum sheet  
13          resistance R;

14          determining number of said contacts N in said sets of  
15          contacts to provide sufficiently low contact resistance  
16          to assure said minimum sheet resistance R dominates

17 total resistance between said first and second sets of  
18 contacts; and

19 defining in said decoupling capacitor contact sites of  
20 sufficient area to accommodate N said contacts with  
21 said first and second sets of said contacts separated  
22 by at least distance K.